which adjoin a surface thereof, which surface is provided with a layer of gate oxide on which gate electrodes are formed at those areas of the semiconductor zones which form gate zones of these transistors, such that the gate electrodes of the PMOS transistors are formed in a layer of p-type doped polycrystalline silicon and a layer of p-type doped polycrystalline silicon-germanium ($Si_{1-x}Ge_x$; $0<x<1$) situated between said polycrystalline silicon layer and the gate oxide, along with an amorphous silicon layer which is formed, characterized in that the gate electrodes of the NMOS transistors are formed in a layer of n-type doped polycrystalline silicon without germanium."

The Office Action states that based on the examples in Hwang, at c. 1, lines 43-50, the PMOS transistors in Hwang are identical to the Applicant's except that Hwang does not disclose polycrystalline silicon without germanium situated in the gate oxide. However, Hwang does not inherently recite Applicant's invention.

Hwang fails to disclose the composition of the gate electrodes of the NMOS transistors formed in the doped n-type layer. Hwang does mention n-type regions can be substituted for p-type regions. However, there is no mention in c. 3 lines 25-40 of an n-type doped polycrystalline silicon without germanium.

In addition, since Hwang mentions that germanium may be used in a p-type region in c. 3 lines 15-20, Hwang would allow germanium to be used in the n-type region. Hwang states that any of the combinations of elements used in the p-type regions can be used in the n-type regions as well (c. 3 lines 31-35). Hwang does not specifically prohibit germanium from being used in the n-type doped layer. Therefore, Hwang fails to recite every element of Claim 1.

Claim 1 states that the "gate electrodes of the NMOS transistors are formed in a layer of n-type doped polycrystalline silicon **without germanium**" (emphasis added). On page 2, line 28 of Applicant's specification, the following is provided: "The use of n-type silicon-germanium gate electrodes in NMOS transistors has only disadvantages. N-type dopants such as arsenic and phosphorus added to silicon-germanium gate electrodes are difficult to activate and are easily deactivated again through heating during treatments carried our subsequently in the manufacturing process at elevated temperatures." The gate zone is largely depleted when these non-activated atoms are present. It is important that the doped n-type layer does not contain germanium otherwise the deleterious effects listed above would occur. Hwang fails to disclose an amorphous layer. Therefore, since Hwang does not disclose every element of Applicant's Claim 1 and reconsideration of this claim is respectfully requested.

Claims 2-4 depend from independent Claim 1 above and are believed patentable for at least the same reasons. However, each is also deemed to define an additional aspect of the invention, and should be individually considered on its own merits.

In addition, Applicant believes the 35 U.S.C. § 103(a) rejection of Claim 3 to be moot in light of the above remarks. Applicant respectfully requests withdrawal of the § 103 rejection.

In view of the foregoing amendments and remarks, it is respectfully submitted that the currently-pending claims are clearly patentably distinguishable over the cited and applied references. Accordingly, entry of this amendment, reconsideration of the rejections of the claims over the references cited, and allowance of this application is earnestly solicited. Applicant's agent can be contacted at the number below.

Respectfully submitted,

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APPENDIX A
MARKED-UP CLAIMS

1. (Amended) A semiconductor device with an integrated CMOS circuit with NMOS and PMOS transistors having semiconductor zones which are formed in a silicon substrate and which adjoin a surface thereof, which surface is provided with a layer of gate oxide on which gate electrodes are formed at those areas of the semiconductor zones which form gate zones of these transistors, such that the gate electrodes of the PMOS transistors are formed in a layer of p-type doped polycrystalline silicon and a layer of p-type doped polycrystalline silicon-germanium ($Si_{1-x}Ge_x$; $0<x<1$) situated between said polycrystalline silicon layer and the gate oxide, along with an amorphous silicon layer which is formed, characterized in that the gate electrodes of the NMOS transistors are formed in a layer of n-type doped polycrystalline silicon without germanium.